

Mixer: Towards Simultaneous Emulation and Virtualization

Master's thesis by Thomas Hütter
Supervised by Univ.-Prof. Dr. Christoph Kirsch

Department of Computer Sciences
Faculty of Natural Sciences
University of Salzburg



Selfie^[1]

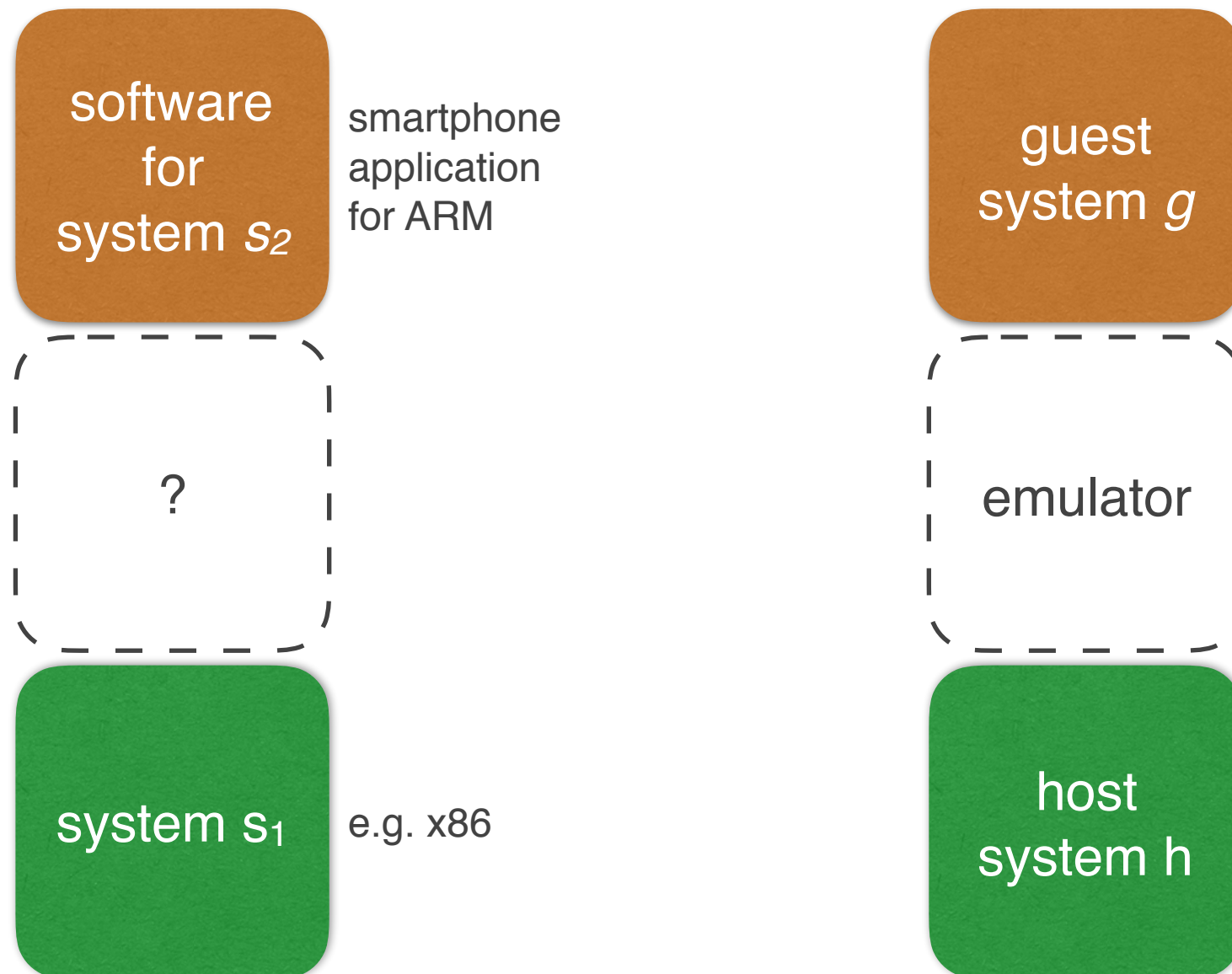
starc
compiler

libcstar
C* library

mipster
emulator

hypster
hypervisor

Emulation



mipster

```
[...]  
lw $t0,-4($fp)  
addiu $t1,$zero,1  
subu $t0,$t0,$t1  
beq $zero,$t0,4[0x238]  
nop  
addiu $t0,$zero,0  
beq $zero,$t0,2[0x23C]  
[...]
```

MIPSter code

MIPSter
machine

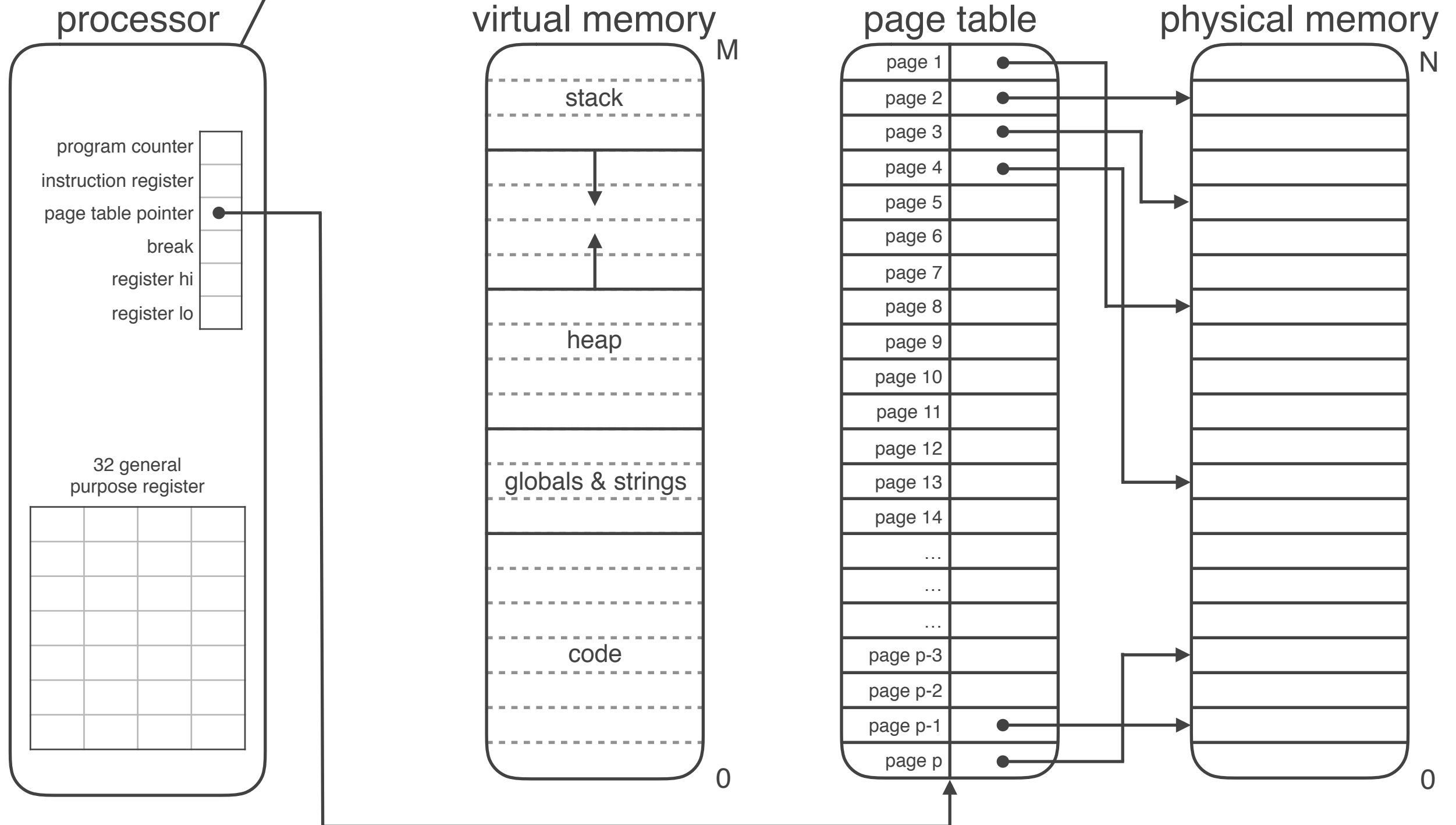
(subset of
MIPS32^[2,3,4])

mipster

host
system h

Emulated machine

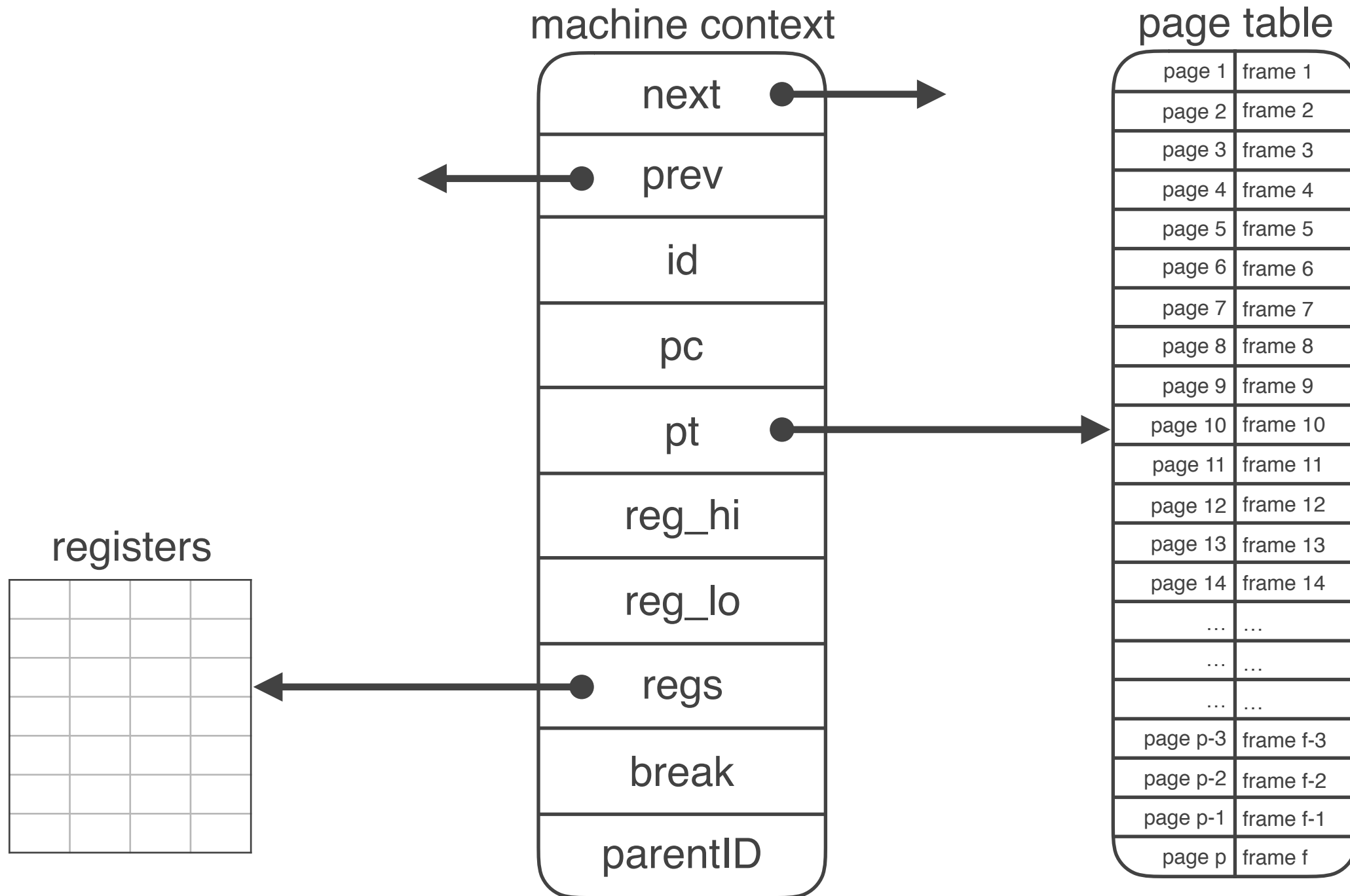
addiu, addu, beq, bne, divu,
j, jal, jr, lw, mfhi, mflo, multu, nop, slt,
subu, sw, syscall



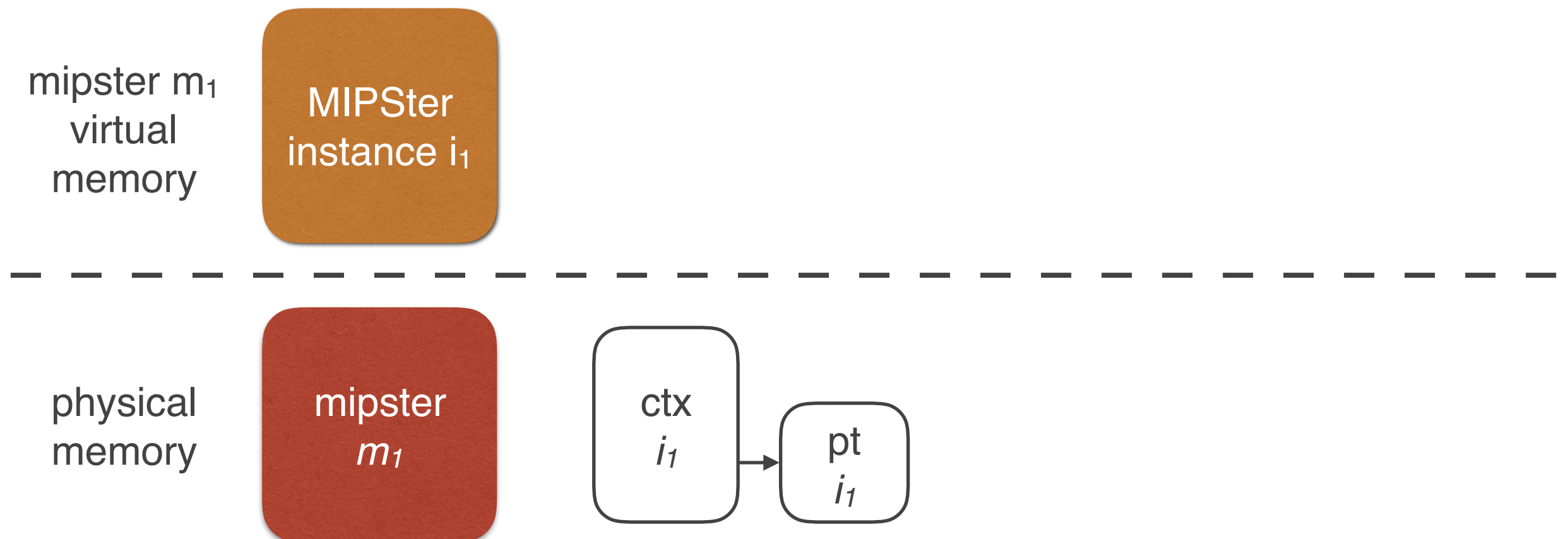
Code interpretation

- **Fetching:** Read an instruction from memory
- **Decoding:** Decode an instruction by a given format
- **Executing:** Perform an instruction

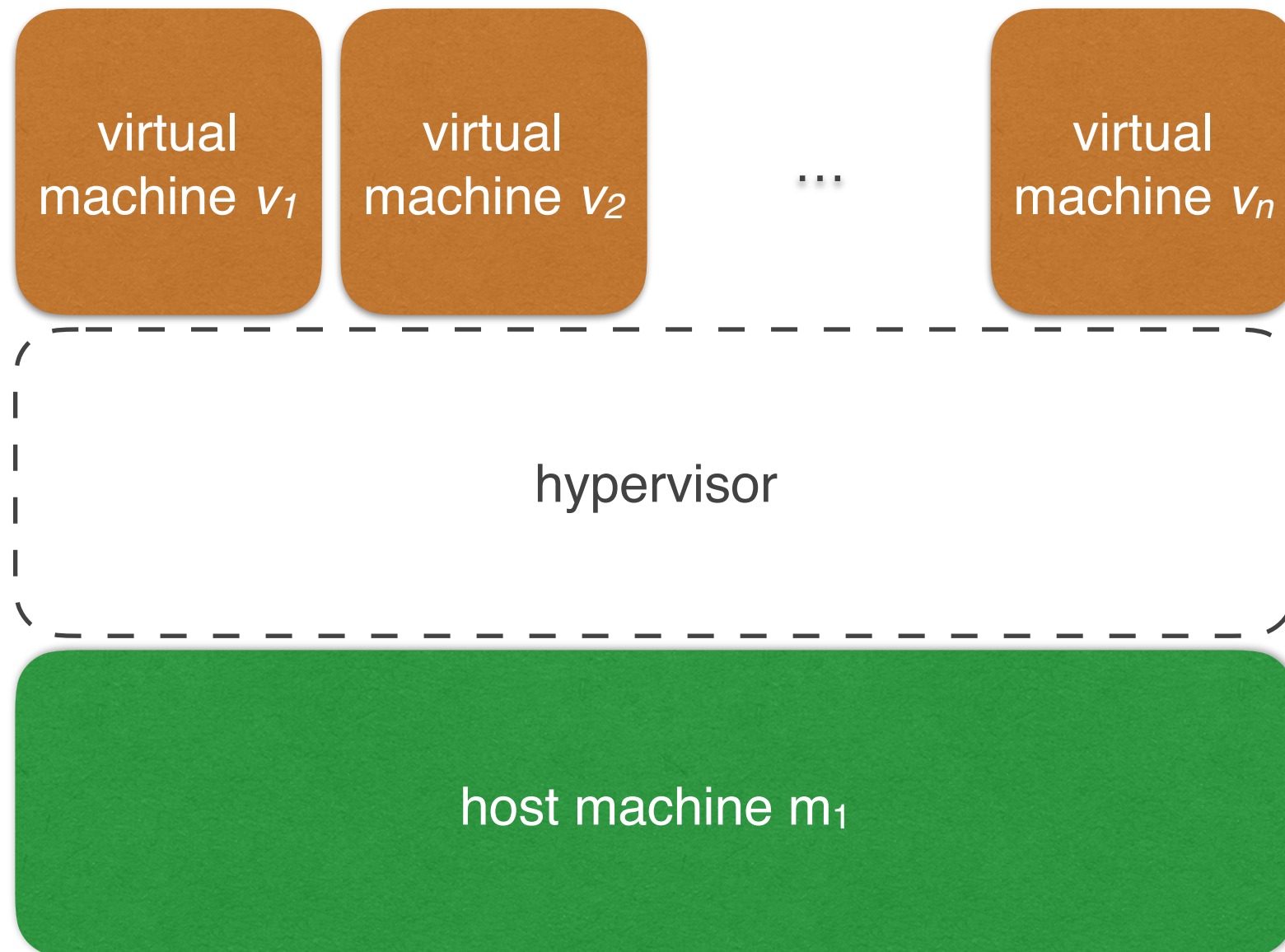
Machine context



Address spaces and machine contexts



Virtualization



hypster

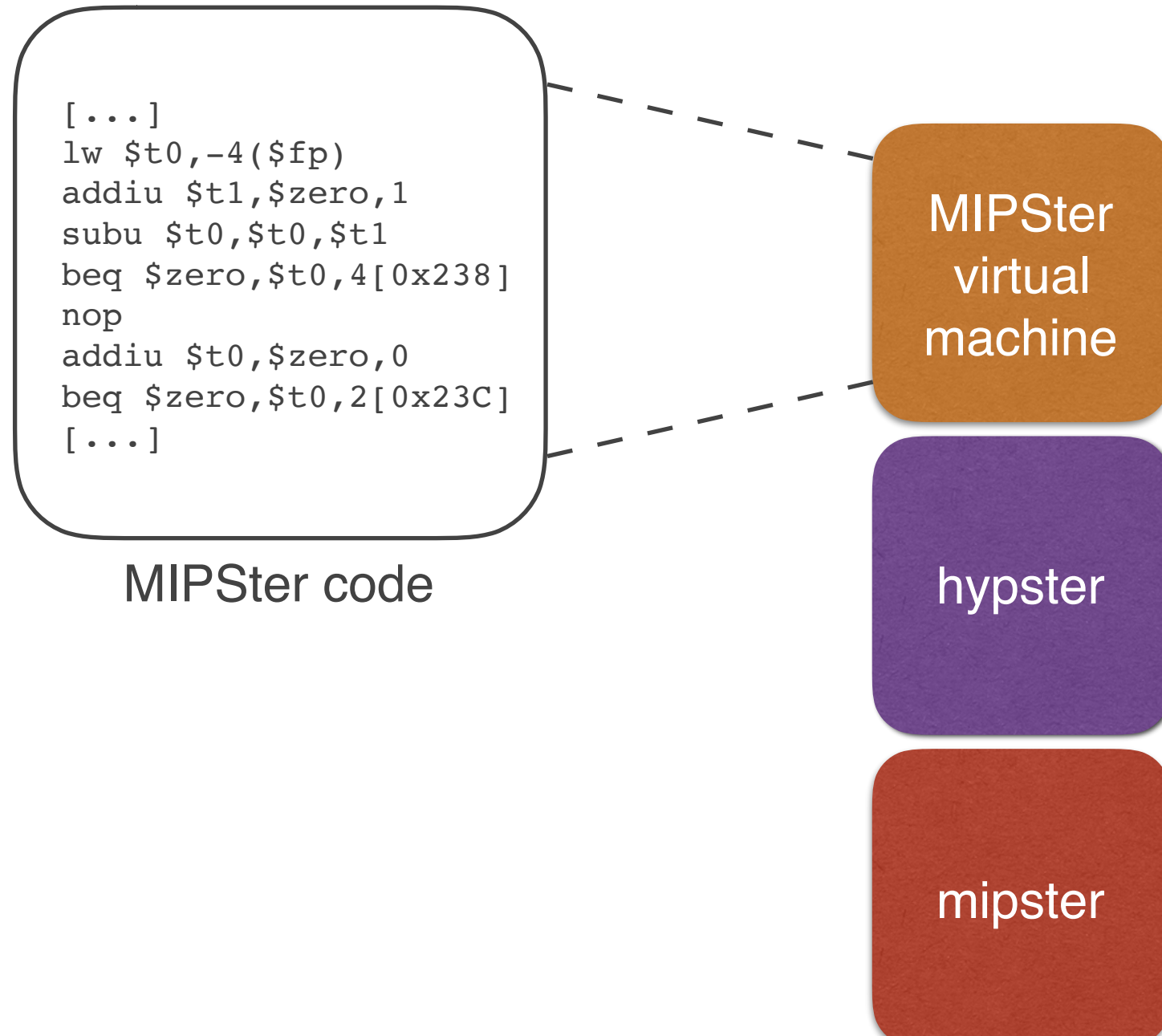
```
[...]  
lw $t0,-4($fp)  
addiu $t1,$zero,1  
subu $t0,$t0,$t1  
beq $zero,$t0,4[0x238]  
nop  
addiu $t0,$zero,0  
beq $zero,$t0,2[0x23C]  
[...]
```

MIPSter code

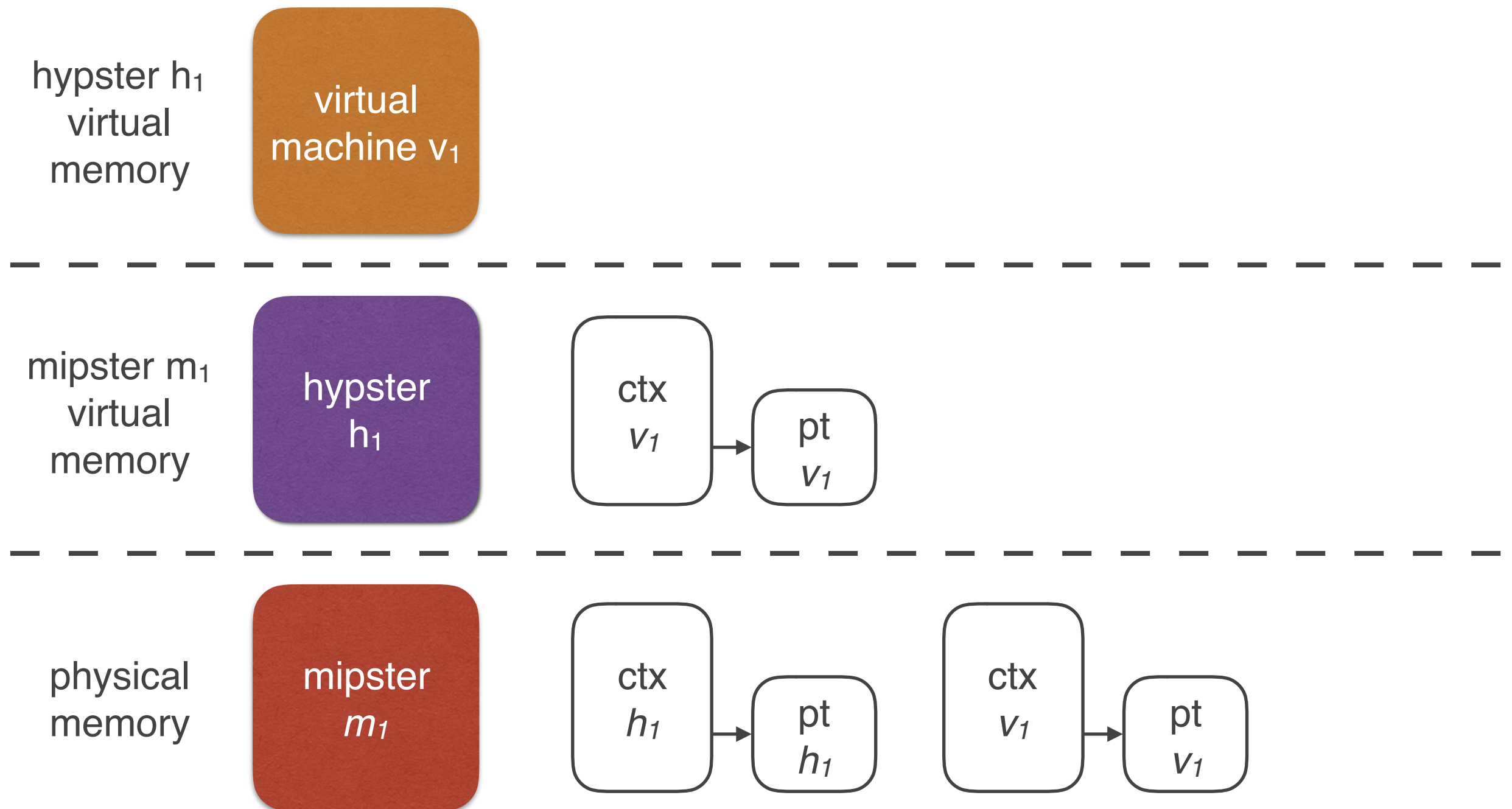
MIPSter
virtual
machine

hypster

mipster



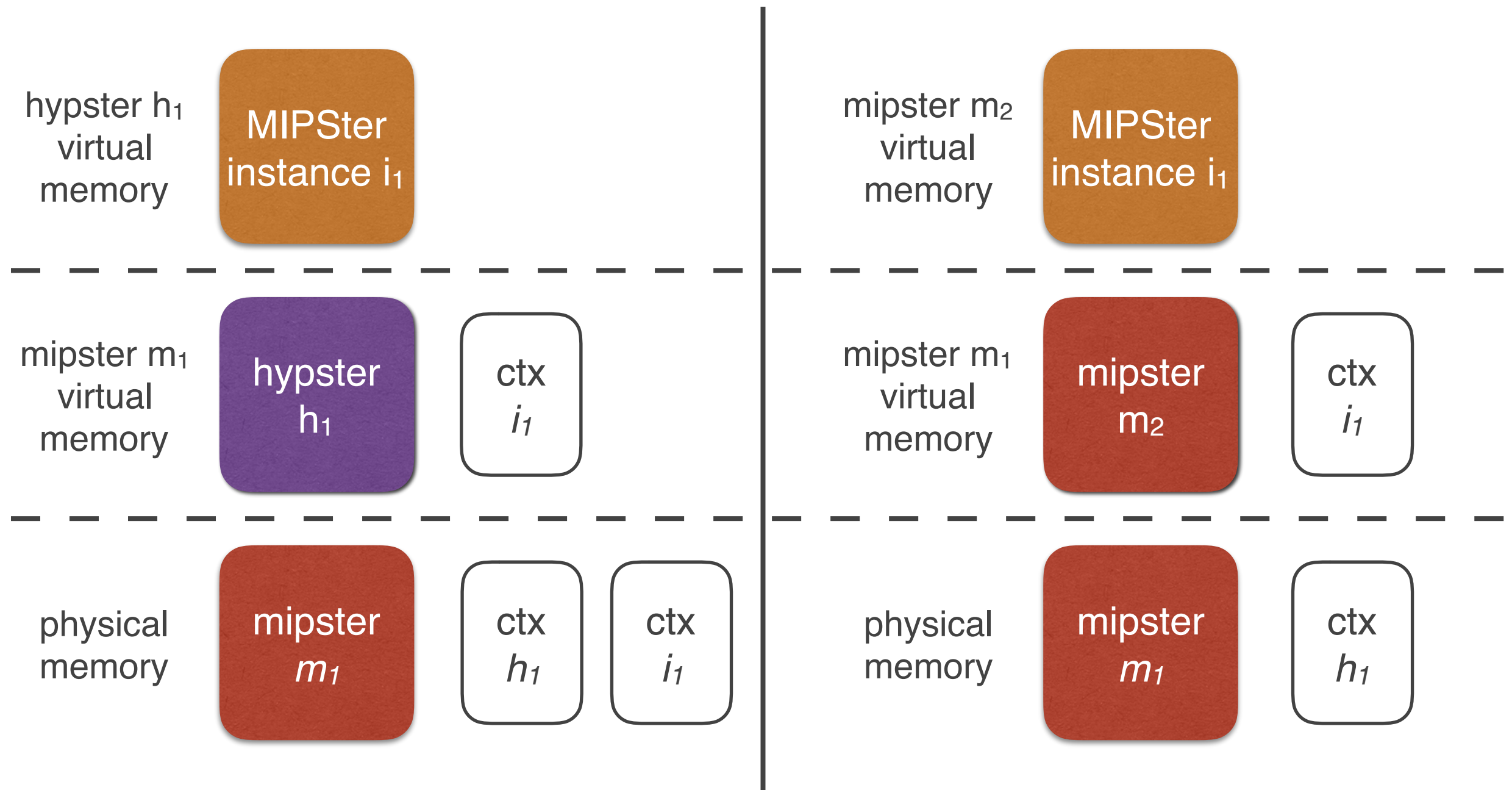
Address spaces and machine contexts



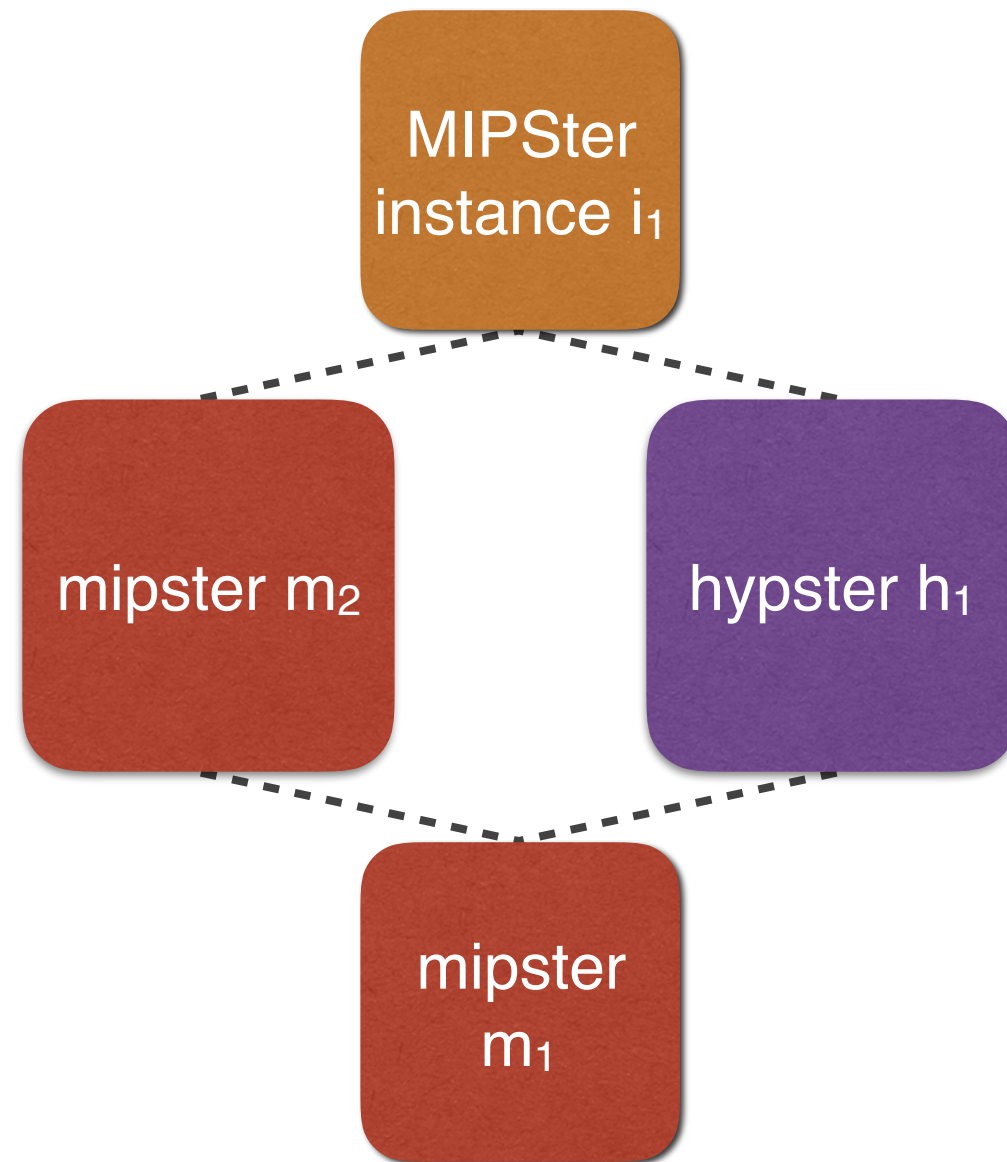
Problem

- Find methods to verify the functional equivalence of emulation and virtualization of the same hardware.

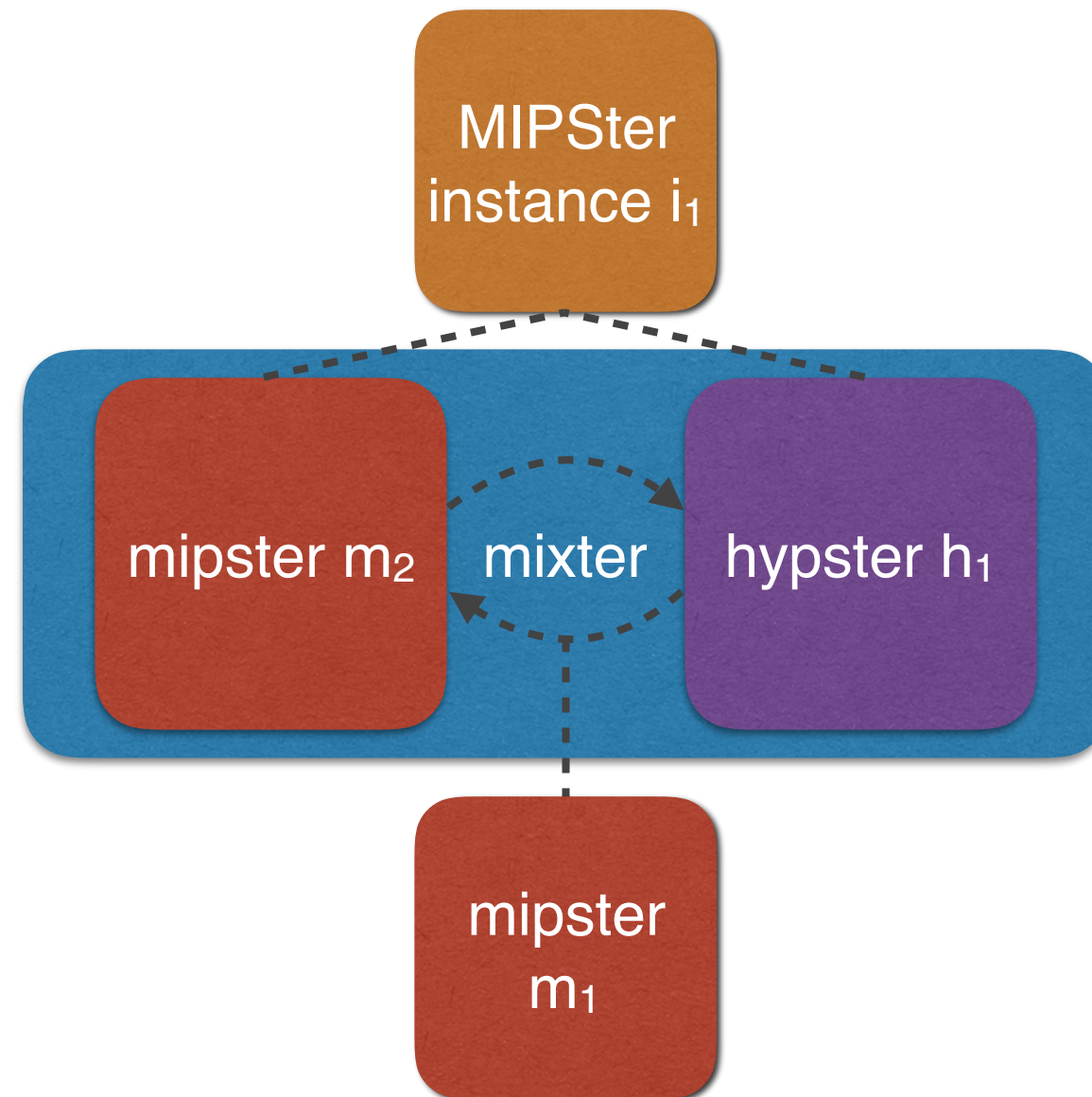
Virtualization and emulation of the same hardware



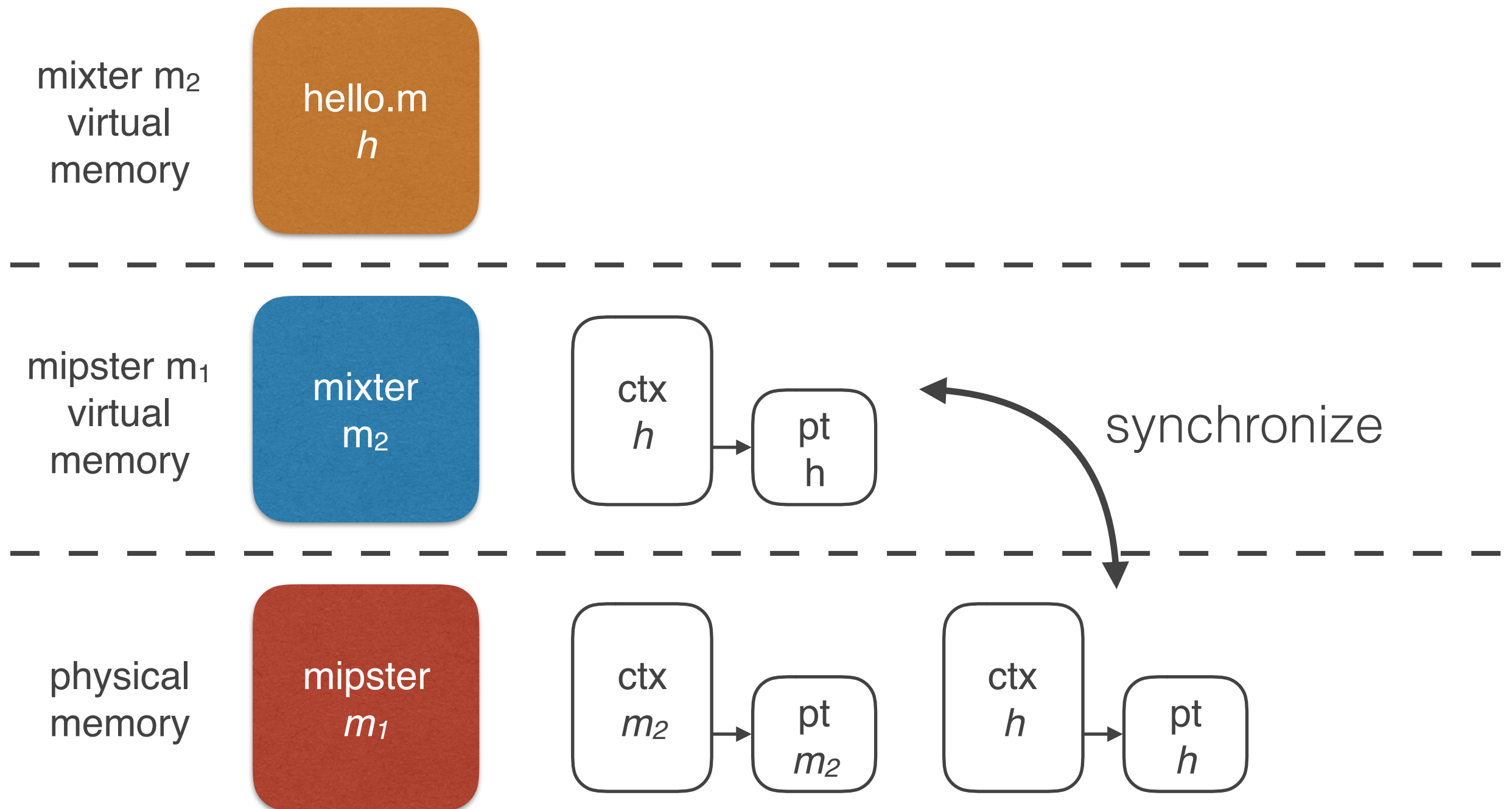
Idea



mixter



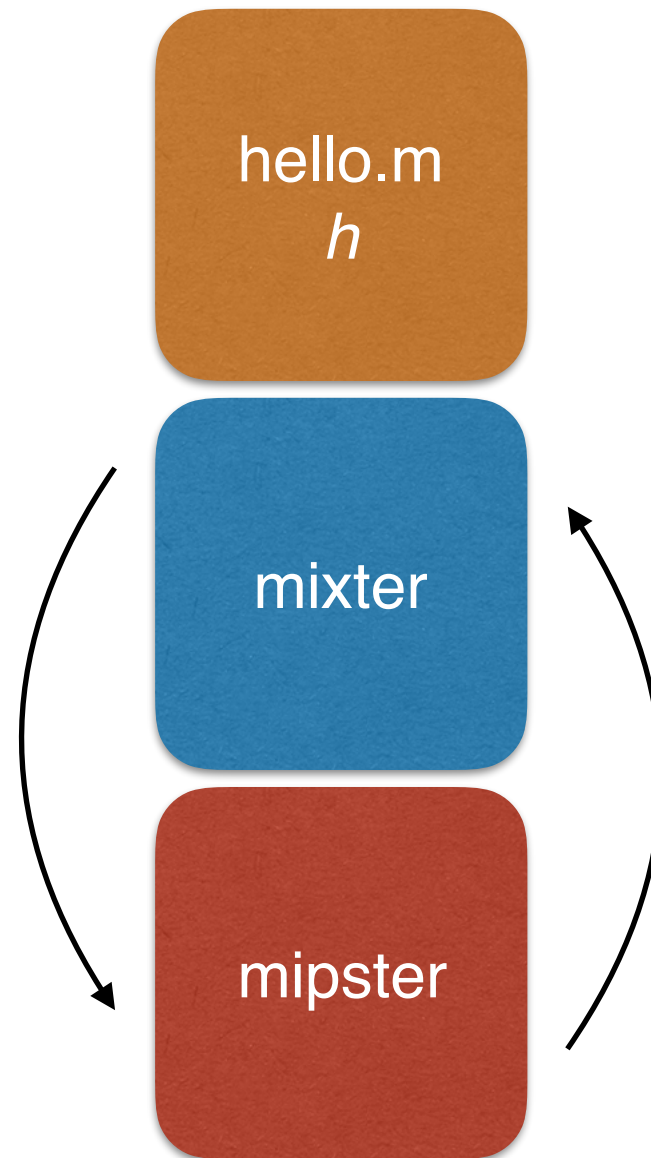
Emulation and Virtualization



Context caching

restoreContext:

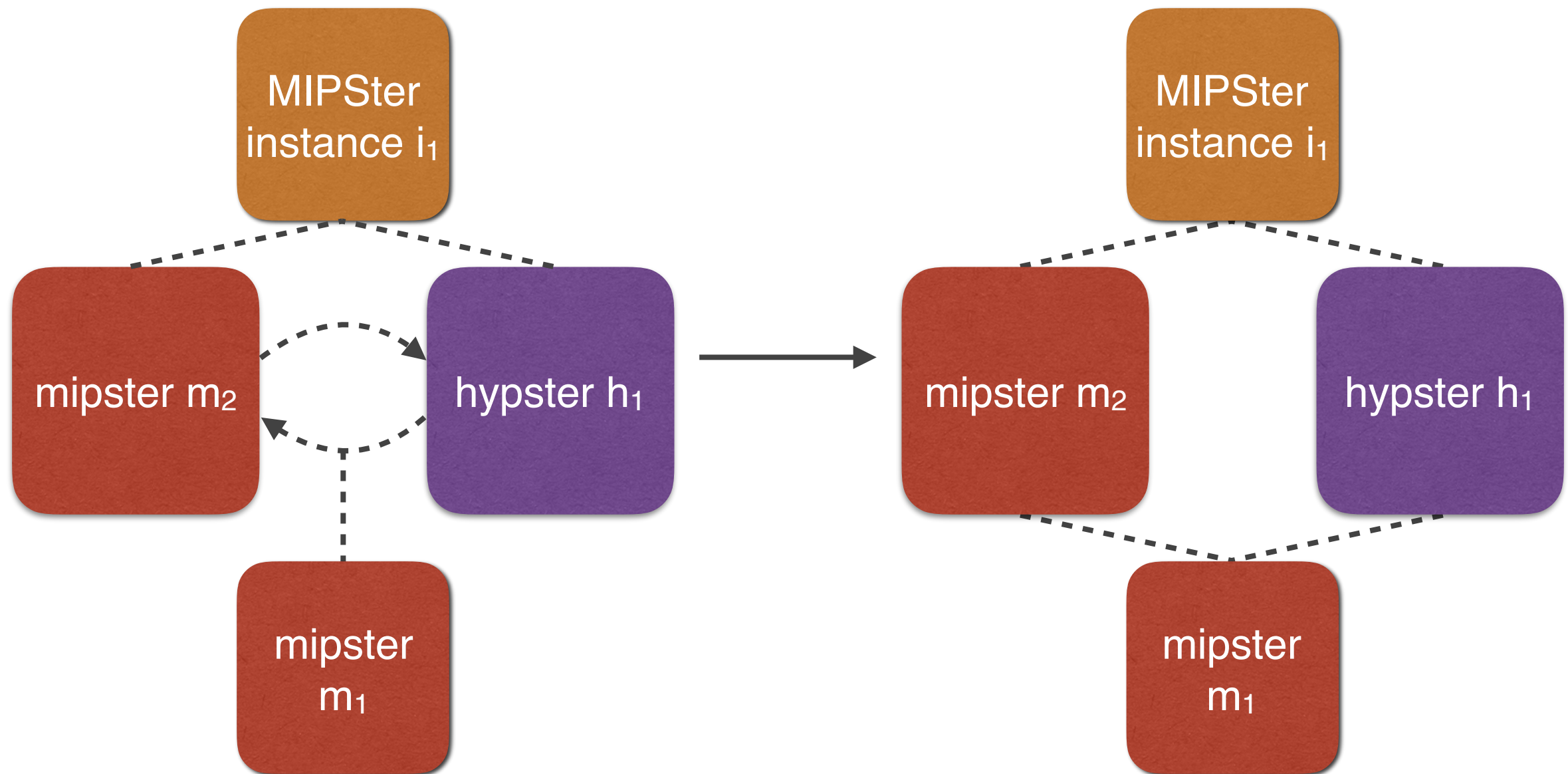
- restore machine state in physical context
 - pc
 - all registers
 - all newly allocated pages



saveContext:

- save machine state in virtual context
 - pc
 - all registers

Future work



References

- [1] Christoph M. Kirsch. Selfie and the basics. In Proceedings of the 2017 ACM International Symposium on New Ideas, New Paradigms, and Reflections on Programming and Software, Onward! 2017. ACM, 2017.
- [2] MIPS Technologies, 1225 Charleston Road, Mountain View, CA. MIPS32 Architecture for Programmers Volume I: Introduction to the MIPS32 Architecture, 0.95 edition, March 2001.
- [3] MIPS Technologies, 1225 Charleston Road, Mountain View, CA. MIPS32 Architecture for Programmers Volume II: The MIPS32 Instruction Set, 0.95 edition, March 2001.
- [4] MIPS Technologies, 1225 Charleston Road, Mountain View, CA. MIPS32 Architecture for Programmers Volume III: The MIPS32 Privileged Resource Architecture, 0.95 edition, March 2001.

Thanks for your
attention!

Any questions?